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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,853	12/02/2003	Scott Fairbanks	6429P001	5587

8791 7590 01/13/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/726,853	FAIRBANKS, SCOTT	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-76* is/are allowed.

6)☒ Claim(s) *1-4,6-14,16 and 18-20* is/are rejected.

7)☒ Claim(s) *5,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features: each of different parts of synchronous logic is coupled through one or more amplifiers to a different one of the clock wires of the clock generator, in claim 6; a plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein the plurality of sets of synchronous logic are interconnected, in claim 11, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bushman et al. (US 6,657,502).

With regard to claim 1, Bushman et al. discloses in Figs. 6-8D an apparatus comprising a clock generator, distributed over an integrated circuit, including a plurality of cells (132', 132'', 134', 134'', 136', 136'', 138', 138'') each coupled to multiple adjacent ones of the plurality of cells by different clock wires, wherein, for each of the plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge.

With regard to claims 2-4 and 10, the reference also meets the recited limitations in these claims.

4. Claims 1, 2, 4, 6-12, 14, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Milshtein et al. (US 6,531,897).

With regard to claim 1, Milshtein et al. discloses in Fig. 1 an apparatus comprising a clock generator, distributed over an integrated circuit, including a plurality of cells (111-113, 106-108) each coupled to multiple adjacent ones of the plurality of cells by different clock wires, wherein, for each of the plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge.

With regard to claims 2, 4 and 10, the reference also meets the recited limitations in these claims.

With regard to claims 6 and 7, each of different parts of synchronous logic (116-123) is coupled through one or more amplifiers to a different one of the clock wires of the clock generator, and wherein the different parts of the synchronous logic are interconnected.

With regard to claims 8 and 9, while the shape is not specifically mentioned, as the claimed structure is met by the prior art, the intended use of the shape of the apparatus is likewise met. Recall that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat App. & Inter. 1987).

With regard to claim 11, Milshtein et al. discloses in Fig. 1 an apparatus comprising a clock generator to generate a clock signal through the interaction of a plurality of cells (111-113, 106-108) distributed in grid over an integrated circuit, wherein each of the plurality of cells is coupled to multiple adjacent complementary ones of the plurality of cells by different clock wires; and a plurality of sets of synchronous logic (116-123) each coupled to a different one of the clock wires, wherein the plurality of sets of synchronous logic are interconnected.

With regard to claims 12, 14, 18 and 19, the reference also meets the recited limitations in these claims.

With regard to claim 20, at least the pull-up type cells or the pull-down type cells include initialization circuitry (134).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Milshtein et al. in view of Graef (US 6,305,001).

The above discussed clock generator circuit of Milshtein et al. meets all of the claimed limitations except for Milshtein et al. does not disclose that the clock grid is three-dimensional. Graef teaches a similar clock generator circuit having three-dimensional grid (see column 13, lines 17-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Graef with the prior art by implementing the clock grid in three-dimensional in order to minimize chip area.

7. Claims 11-14, 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bushman et al. in view of Potter et al. (US 6,118,304).

With regard to claim 11, Bushman et al. discloses in Figs. 6-8D an apparatus comprising a clock generator to generate a clock signal through the interaction of a plurality of cells (132', 132'', 134', 134'', 136', 136'', 138', 138'') distributed in grid over an integrated circuit, wherein each of the plurality of cells is coupled to multiple adjacent complementary ones of the plurality of cells by different clock wires. The apparatus of Bushman et al. meets all of the claimed limitations of claim 11 except for a plurality of sets of synchronous logic each coupled to a different one of the clock wires, which is considered to be an intended use. Potter et al. teaches

in Figs. 18-20 a method and apparatus for logic synchronization by using the multi-phase clock signals, which are similar to clock signals of Bushman et al., to drive a plurality of sets of synchronous logic. Therefore, it would have been obvious to one of ordinary skill in the art to realize that the clock signals of Bushman et al. can be used to drive the plurality of sets of synchronous logic in order to provide the synchronization to the apparatus.

With regard to claims 12-14, 16, 18, and 19, the references also meet the recited limitations in these claims.

Allowable Subject Matter

8. Claims 5, 15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest an apparatus (as shown in Fig. 4), as recited in claims 5 and 15, having specific structural limitations such as each of the plurality of cells (401-416) to detect a plurality of clock edges (N, S, E, W in instant Fig. 2A) being currently generated by the clock generator and trigger a next clock edge based on arrival times of the detected plurality of clock edges.

Claim 17 is allowed for similar reasons; note the above discussion with regard to claims 5 and 15.

9. Claims 21-76 are allowed.

The prior art of record fails to disclose or fairly suggest a clock generator (as shown in Fig. 7), as recited in claim 21, having specific structural limitations such as including a plurality of cells (701-716) distributed in grid over an integrated circuit that collectively form an oscillator

of the clock generator, wherein each of the plurality of cells (i.e. 702) oscillate dependent upon clock signals received from multiple of others of the plurality of cells (701, 703); and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a distributed clock generator (as shown in Fig. 7), as recited in claim 30, having specific structural limitations such as comprising a plurality of cells (701-716) that, responsive (i.e. 702) to an averaging of a previous clock edge produced by the plurality of cells (701, 703), detect when to produce the next clock edge, and a plurality of clock wires each coupling together two of the plurality of cells such that the plurality of cells are coupled together in grid; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a distributed clock generator (as shown in Fig. 7), and a method of use thereof, as recited in claims 39 and 75, having specific structural limitations such as comprising a plurality of cells (701-716) each including, a plurality of terminals, a cumulative clock edge detection circuit (601-604 in instant Fig. 6) coupled to the plurality of terminals and having an output (605), a delay/amplification circuit (606-608) coupled to the output of the cumulative clock edge detection circuit, and a driver circuit (609-612) coupled to the plurality of terminals and to the delay/amplification circuit; a plurality of clock wires, each of the plurality of clock wires coupling one of the plurality of terminals of one of the plurality of cells to one of the plurality of terminals of another of the plurality of cells.

The prior art of record fails to disclose or fairly suggest a distributed clock generator (as shown in Fig. 7), as recited in claim 52, having specific structural limitations such as comprising

a plurality of cells (701-716) collectively having a plurality of terminal pairs, each of the plurality of terminal pairs (inputs of 601 & 603, and 602 & 604) including a charging terminal (inputs of 601 and 602) coupled to a discharging terminal (inputs of 603 and 604) to have generated there between a clock signal (605) having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal, the terminals of each of the plurality of terminal pairs being part of two different ones of the plurality of cells, the plurality of cells coupled together as a result of each being coupled to certain others of the plurality of cells by the plurality of terminal pairs; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a cell (as shown in Fig. 6) of distributed clock generator (Fig. 7), as recited in claim 62, having specific structural limitations such as comprising a set of terminals of the cell, each of the terminals in the set being one terminal of a different terminal pair, each of the terminal pairs (inputs of 601 & 603, and 602 & 604) including a charging terminal (inputs of 601 and 602) coupled to a discharging terminal (inputs of 603 and 604) to have generated there between a clock signal (605) having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal; a cumulative clock edge detection circuit (601-604) coupled to the set of terminals to determine a single clock edge transition time reflective of transitions of the clock signals on the terminals, a driver circuit (609-612) coupled to the set of terminals; and a delay/amplification circuit (606-608), coupled to an output of the cumulative clock edge detection circuit and to the driver circuit, to cause another clock edge transition of the clock signals to substantially simultaneously occur some delay time after each of the single clock edge transition times.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Masleid (US Pat. 6,701,444) is cited as of interest because it discloses a method and apparatus for process independent clock signal distribution circuit.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
December 29, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800